CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a ferroelectric capacitor comprising:

a conductive lower electrode material formed above a semiconductor body;

a ferroelectric material formed above the lower electrode material, the ferroelectric material comprising unit cells individually comprising an elongated dimension, wherein a percentage of the unit cells are oriented with elongated dimensions substantially normal to a generally planar upper surface of the semiconductor body, and wherein the percentage is about 50% or more and about 90% or less; and

a conductive upper electrode material formed above the ferroelectric material.

2. The device of claim 1, wherein the ferroelectric material comprises PZT.

3. The device of claim 2, wherein the percentage is about 60% or more and about 70% or less.

4. The device of claim 2, wherein the lower electrode material comprises Iridium.

5. The device of claim 2, wherein the percentage is about 50% or more and about 70% or less.

6. The device of claim 2, wherein the unit cells of the ferroelectric material have a tetragonal distortion of about 1% or more and about 4% or less.

7. The device of claim 2, wherein the PZT ferroelectric material comprises a Zr content of about 0-52%.

8. The device of claim 7, wherein the PZT ferroelectric material comprises a Zr content of about 10-40%.

9. The device of claim 1, wherein the percentage is about 60% or more and about 70% or less.

10. The device of claim 9, wherein the lower electrode material comprises Iridium.

11. The device of claim 9, wherein the percentage is about 50% or more and about 70% or less.

12. The device of claim 1, wherein the lower electrode material comprises Iridium.

13. The device of claim 1, wherein the percentage is about 50% or more and about 70% or less.

14. The device of claim 1, wherein the unit cells of the ferroelectric material have a tetragonal distortion of about 1% or more and about 4 % or less.

15. A ferroelectric capacitor comprising:

a conductive lower electrode material formed above the semiconductor body;

a ferroelectric material formed above the lower electrode material, the ferroelectric material comprising unit cells individually comprising an elongated dimension; and

a conductive upper electrode material formed above the ferroelectric material;

wherein the upper and lower electrodes are spaced from one another along an axis, wherein a percentage of the unit cells in the ferroelectric material are oriented with elongated dimensions substantially parallel to the axis, and wherein the percentage is about 50% or more and about 90% or less.

16. The ferroelectric capacitor of claim 15, wherein the ferroelectric material comprises PZT.

17. The ferroelectric capacitor of claim 16, wherein the percentage is about 60% or more and about 70% or less.

18. The ferroelectric capacitor of claim 16, wherein the lower electrode material comprises Iridium.

19. The ferroelectric capacitor of claim 16, wherein the percentage is about 50% or more and about 70% or less.

20. The ferroelectric capacitor of claim 16, wherein the unit cells of the ferroelectric material have a tetragonal distortion of about 1% or more and about 4% or less.

21. The ferroelectric capacitor of claim 16, wherein the PZT ferroelectric material comprises a Zr content of about 0-52%.

22. The ferroelectric capacitor of claim 16, wherein the PZT ferroelectric material comprises a Zr content of about 10-40%.

23. The ferroelectric capacitor of claim 15, wherein the percentage is about 60% or more and about 70% or less.

24. The ferroelectric capacitor of claim 23, wherein the lower electrode material comprises Iridium.

25. The ferroelectric capacitor of claim 23, wherein the percentage is about 50% or more and about 70% or less.

26. The ferroelectric capacitor of claim 15, wherein the lower electrode material comprises Iridium.

27. The ferroelectric capacitor of claim 15, wherein the percentage is about 50% or more and about 70% or less.

28. A method of fabricating a ferroelectric capacitor in a wafer, the method comprising:

forming a lower electrode material above a semiconductor body in the wafer;

forming a ferroelectric material above the lower electrode material, the ferroelectric material comprising unit cells individually comprising an elongated dimension, wherein a percentage of the unit cells are oriented with elongated dimensions substantially normal to an upper surface of the semiconductor body, and wherein the percentage is about 50% or more and about 90% or less;

forming an upper electrode material above the ferroelectric material; and

etching portions of the upper electrode material, the ferroelectric material, and the lower electrode material to form a ferroelectric capacitor.

29. The method of claim 28, wherein forming the ferroelectric material comprises:

preheating the wafer in a substantially non-oxidizing ambient with no precursor gases flowing; and

depositing the ferroelectric material over the lower electrode material after preheating the wafer.

30. The method of claim 29, wherein the substantially non-oxidizing ambient comprises Argon.

31. The method of claim 30, wherein preheating the wafer comprises preheating the wafer at a pressure of about 8 Torr in the non-oxidizing ambient.

32. The method of claim 31, wherein depositing the ferroelectric material comprises performing a deposition process at a pressure of about 8 Torr to form the ferroelectric material above the lower electrode material.

33. The method of claim 30, wherein depositing the ferroelectric material comprises performing a deposition process at a pressure of about 8 Torr to form the ferroelectric material above the lower electrode material.

34. The method of claim 29, wherein preheating the wafer comprises preheating the wafer at a pressure of about 8 Torr in the non-oxidizing ambient.

35. The method of claim 34, wherein depositing the ferroelectric material comprises performing a deposition process at a pressure of about 8 Torr to form the ferroelectric material above the lower electrode material.

36. The method of claim 29, wherein depositing the ferroelectric material comprises performing a deposition process at a pressure of about 8 Torr to form the ferroelectric material above the lower electrode material.

37. The method of claim 29, wherein depositing the ferroelectric material comprises performing a metal organic chemical vapor deposition process to form the ferroelectric material over the lower electrode material.

38. The method of claim 28, wherein forming the ferroelectric material comprises performing a metal organic chemical vapor deposition process to form the ferroelectric material over the lower electrode material.

39. The method of claim 38, wherein forming the ferroelectric material comprises performing the metal organic chemical vapor deposition process at a pressure of about 8 Torr.

40. The method of claim 28, wherein forming the ferroelectric material comprises depositing the ferroelectric material above the lower electrode material at a pressure of about 8 Torr.

41. The method of claim 28, wherein forming the ferroelectric material comprises depositing PZT material above the lower electrode material.

42. The method of claim 41, wherein forming the ferroelectric material comprises performing a metal organic chemical vapor deposition process to form the PZT material over the lower electrode material.

43. The method of claim 42, wherein forming the ferroelectric material comprises performing the metal organic chemical vapor deposition process at a pressure of about 8 Torr.

44. The method of claim 41, wherein the forming the lower electrode material comprises forming Iridium above the semiconductor body.

45. The method of claim 41, wherein the unit cells of the ferroelectric material have a tetragonal distortion of about 1% or more and about 4% or less.

46. The method of claim 41, wherein the PZT ferroelectric material comprises a Zr content of about 0-52%.

47. The method of claim 46, wherein the PZT ferroelectric material comprises a Zr content of about 10-40%.

48. The method of claim 28, wherein the forming the lower electrode material comprises forming Iridium above the semiconductor body.

49. The method of claim 28, wherein the percentage is about 50% or more and about 70% or less.

50. The method of claim 28, wherein the percentage is about 60% or more and about 70% or less.